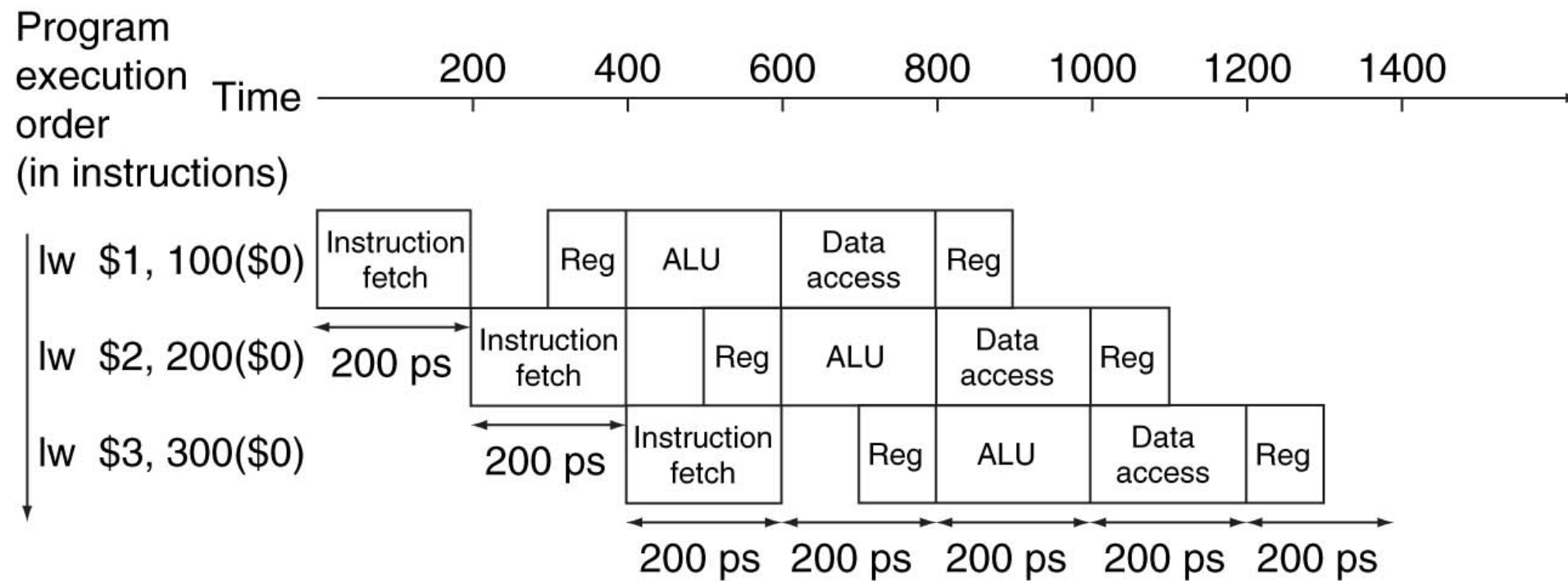
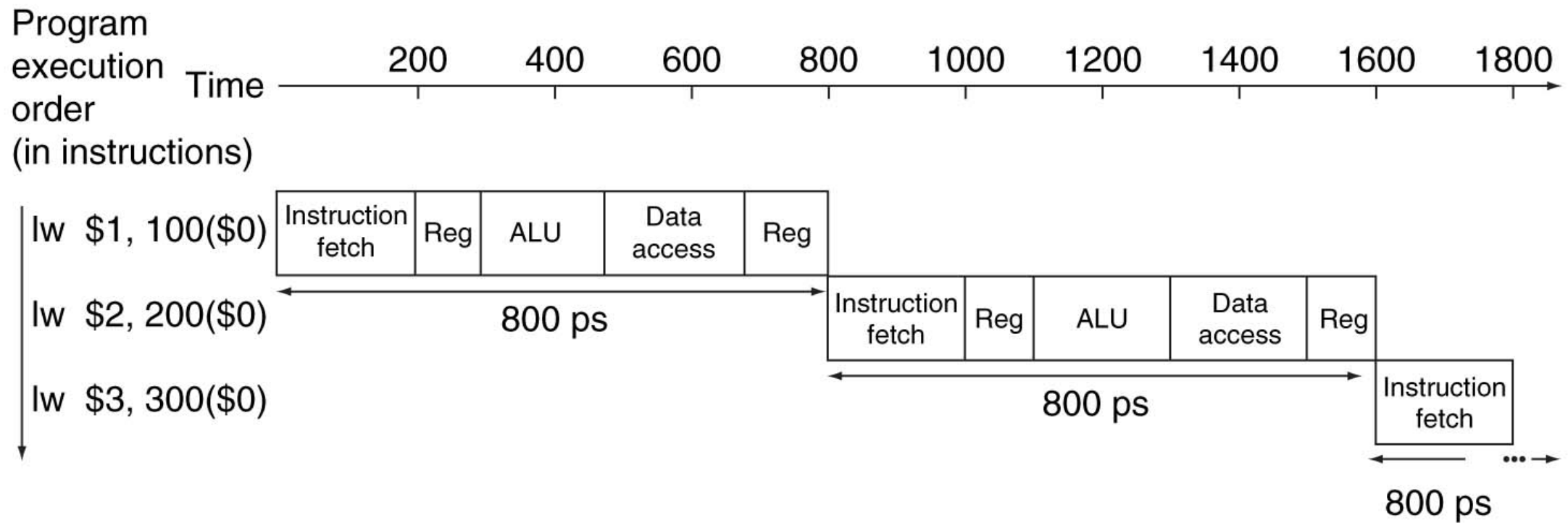


# CSCI341

## Lecture 34, Pipelined Datapath

# RECALL...

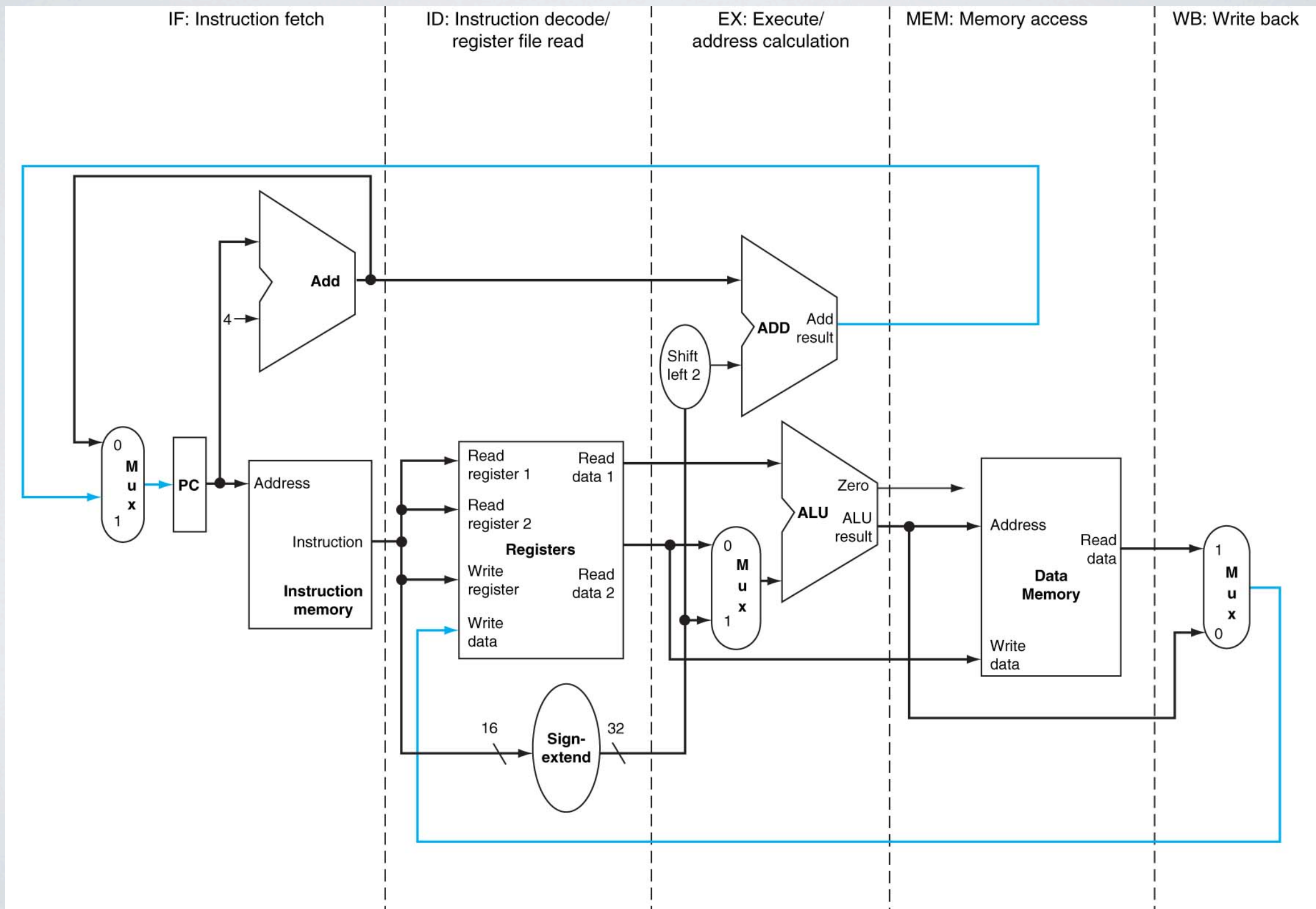


# RECALL...

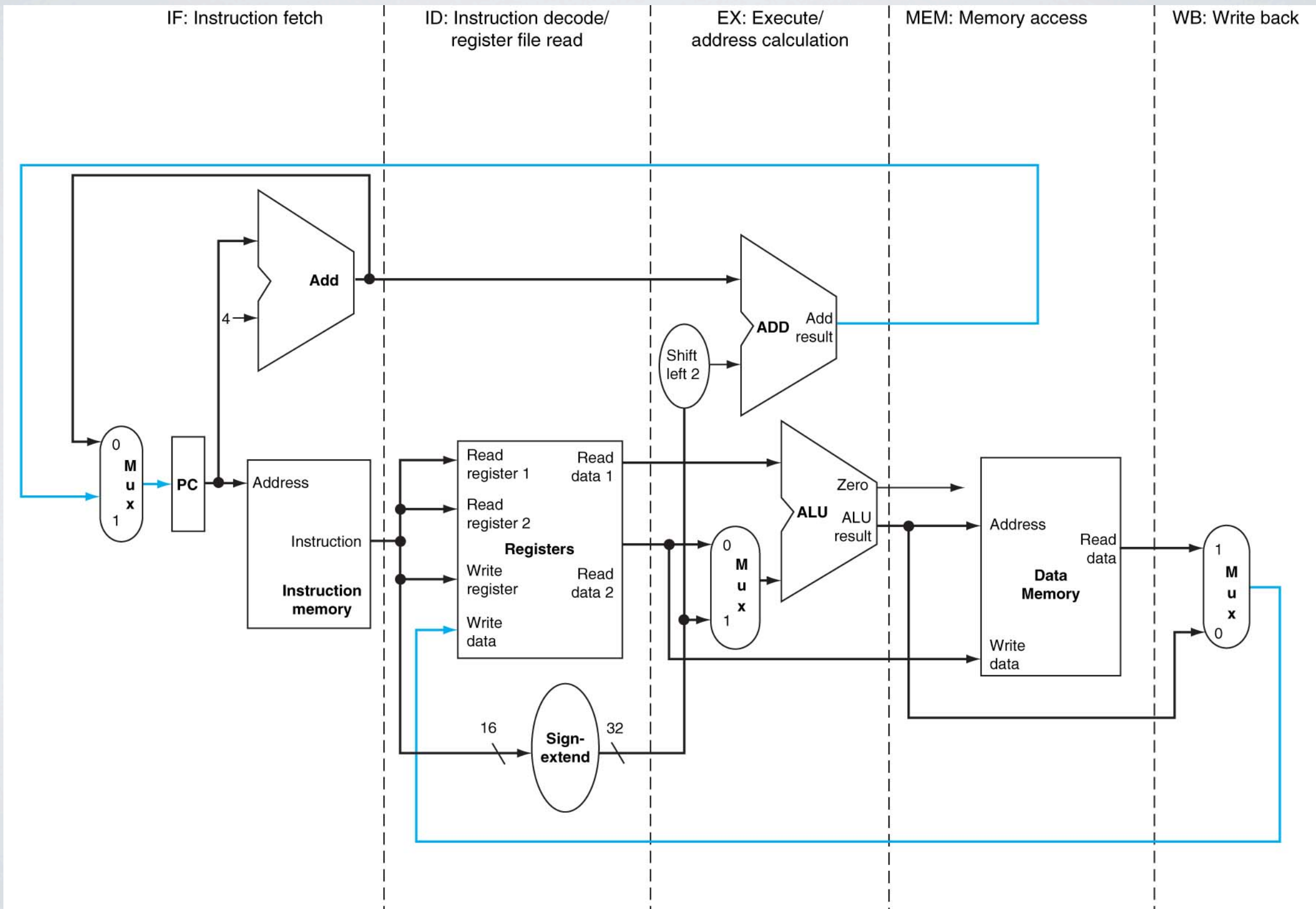
- Structural Hazards
- Data Hazards
- Control Hazards



# SINGLE-CYCLE DATAPATH



# LEFT TO RIGHT



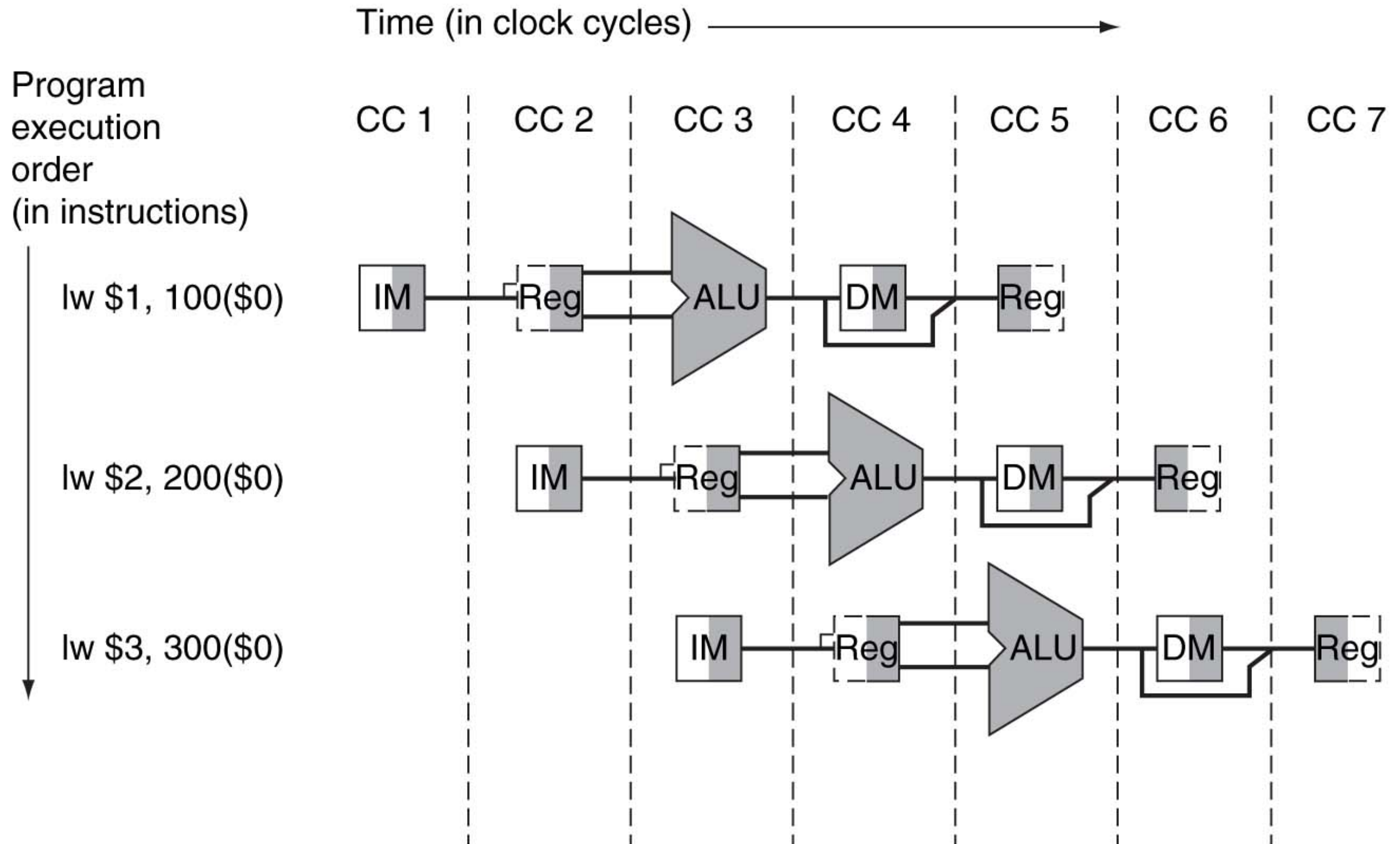
# EXCEPT... LEFT-TO-RIGHT

- Writing back to the register file (what kind of hazard?)
- Selecting the value of PC (what kind of hazard?)

Note that data flowing R-to-L doesn't affect the *current* instruction.



# PIPELINED EXECUTION (PRETEND)



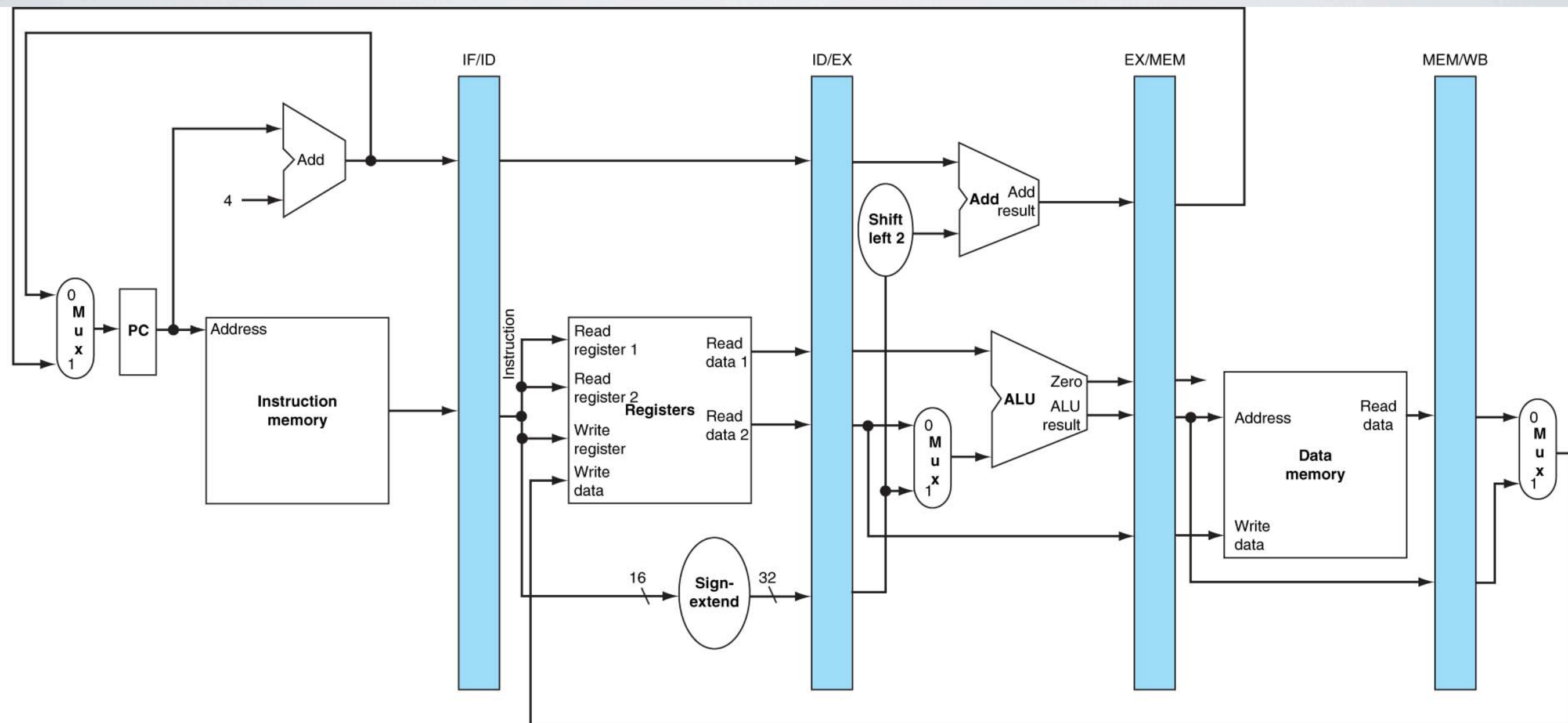
# PIPELINE REGISTERS

64 bits

128 bits

97 bits

64 bits





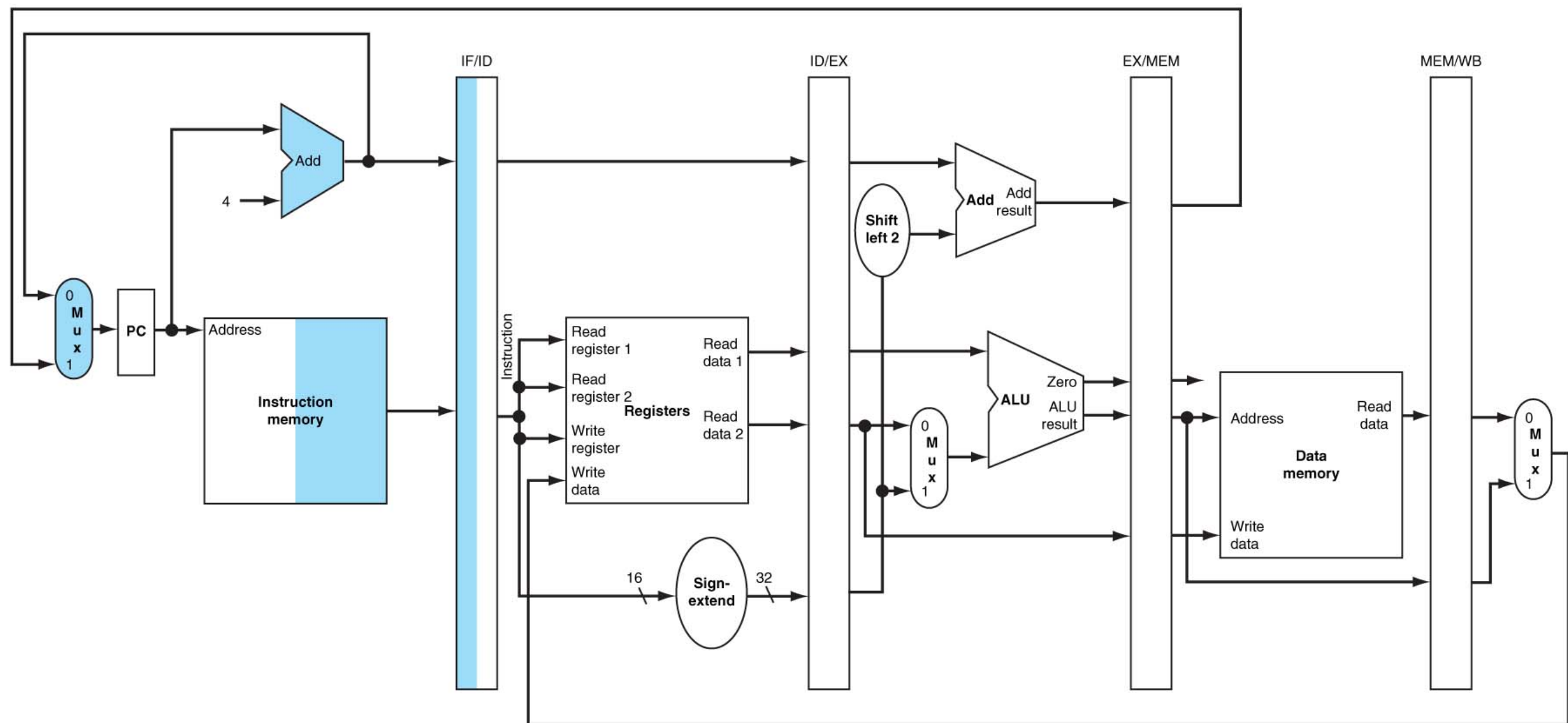
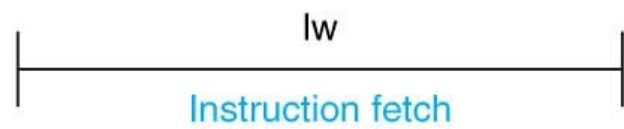
# EXAMPLE

Five stages of a `lw` instruction.

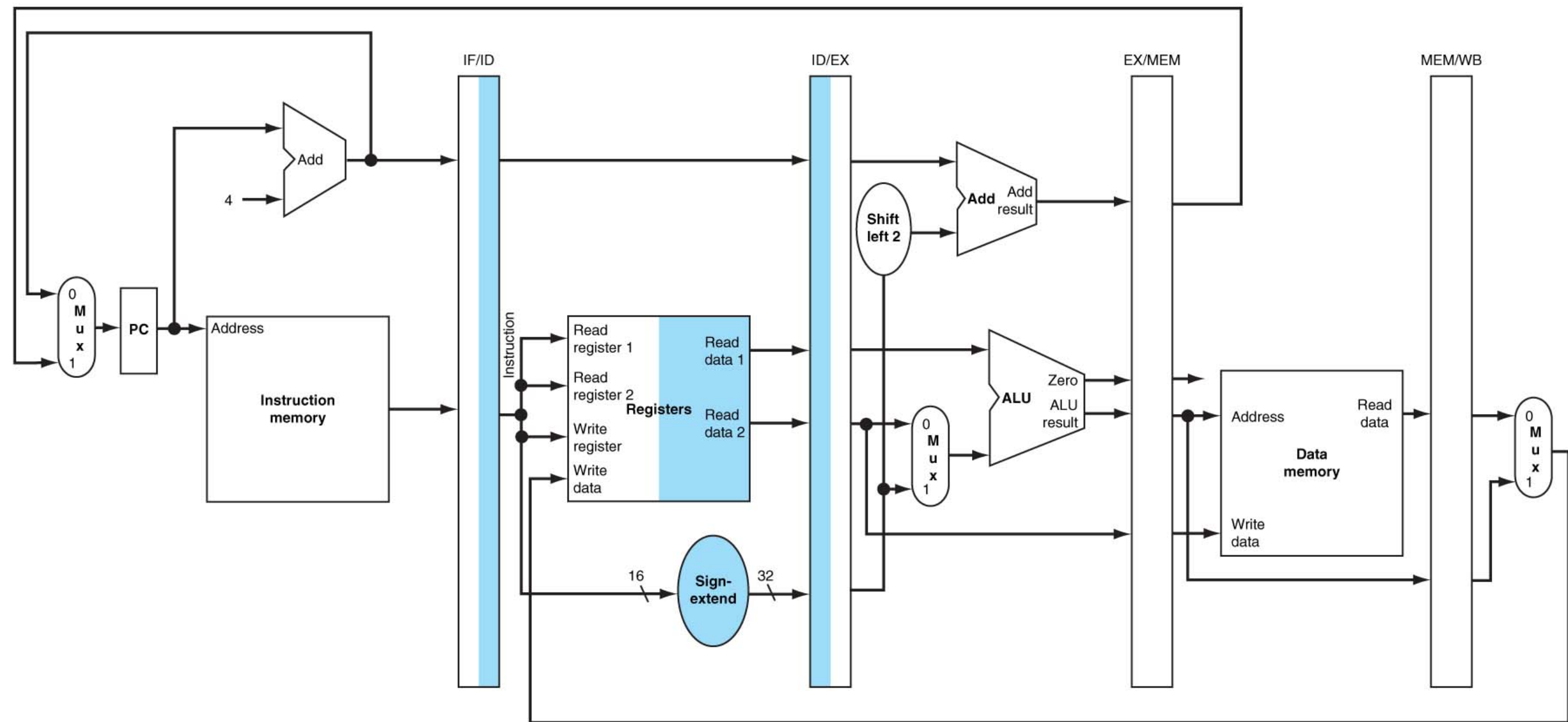
Note:

shaded on the right: read

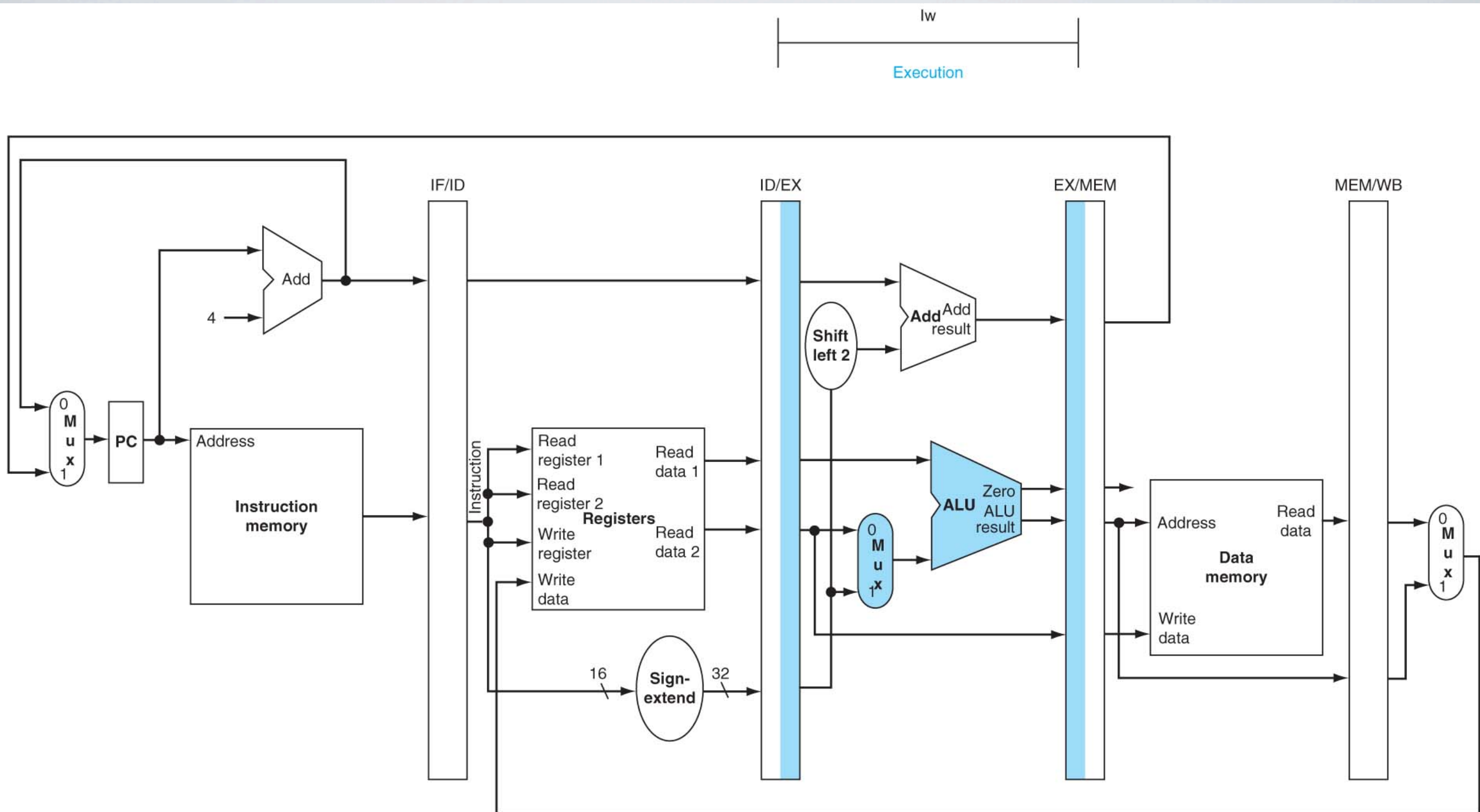
shaded on the left: write

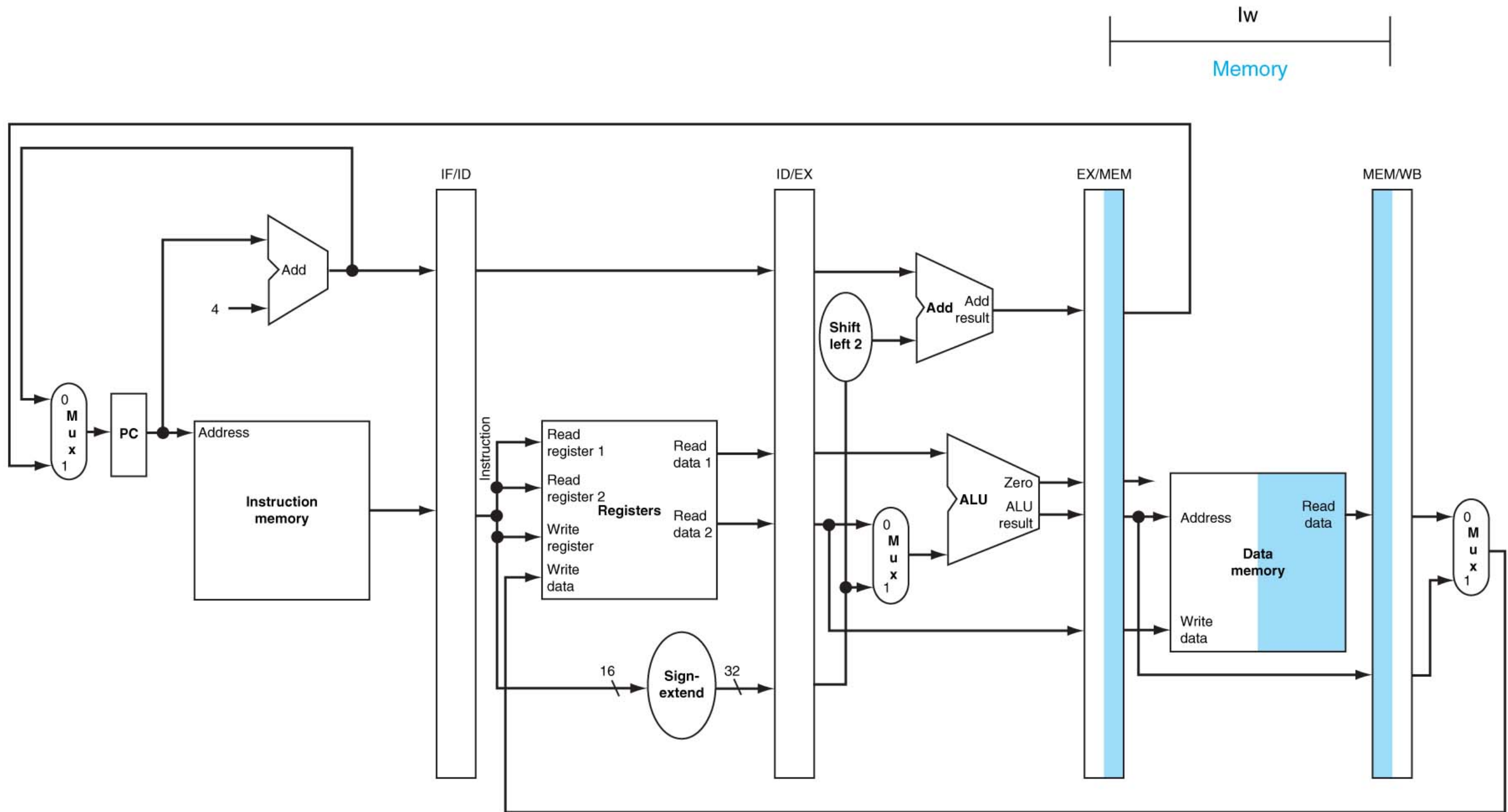


lw  
Instruction decode

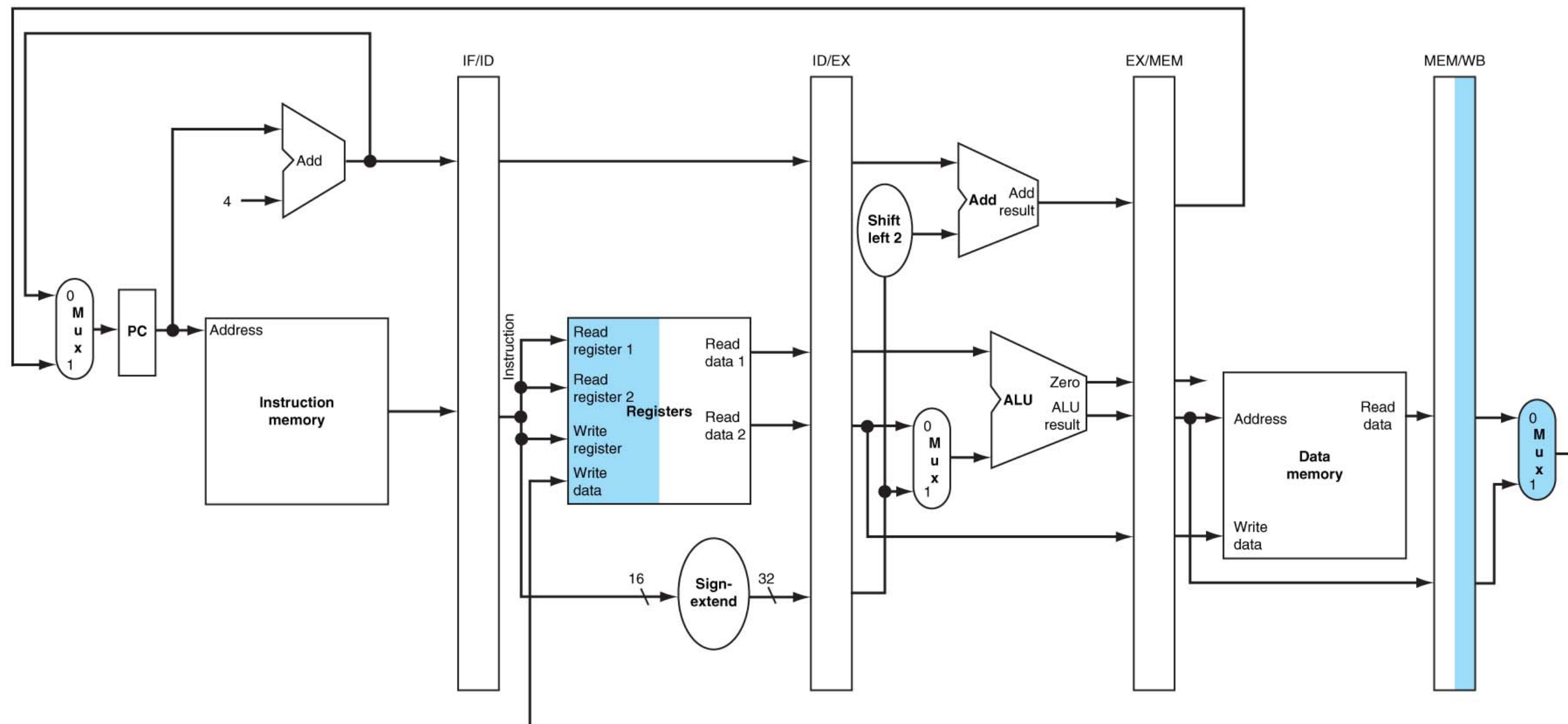








lw  
Write-back





# HOMEWORK

- Reading 29



I zombies.